Intel® 41210 Serial to Parallel PCI Bridge Evaluation Board

User's Guide

October 2004

Order Number: 278947-002

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Revision History

Date	Revision	Description
October 2004	002	-Updated naming terminology in Sections 2.0 and 3.0. -Corrected PCI Bus name Header Connectors J5 and J6 in Section 4.0. -Corrected Switch S3 and S4 PCI-X 66 MHZ Pos 3 settings in Table 1.
December 2003	001	This is the first release of this document.

1.0 Introduction

This document describes the Intel® 41210 Serial to Parallel PCI Bridge (also called 41210 Bridge) Evaluation Board.

2.0 Overview

The Intel® 41210 Serial to Parallel PCI Bridge evaluation board is a PCI-Express enabling tool with PCI-X expansion slots that are used to evaluate the operation of the 41210 Bridge. The 41210 Bridge evaluation board can be used to perform the following functions:

- Develop initialization code to configure the 41210 Bridge and associated logic and devices on the local PCI-X bus as a intelligent controller.
- Evaluate the operation of the 41210 Bridge with a variety of PCI/PCI-X devices configured in an intelligent subsystem.
- Build and evaluate a system.
- Testing of the 41210 Bridge feature set.

3.0 Features

The 41210 Bridge evaluation board has the following features:

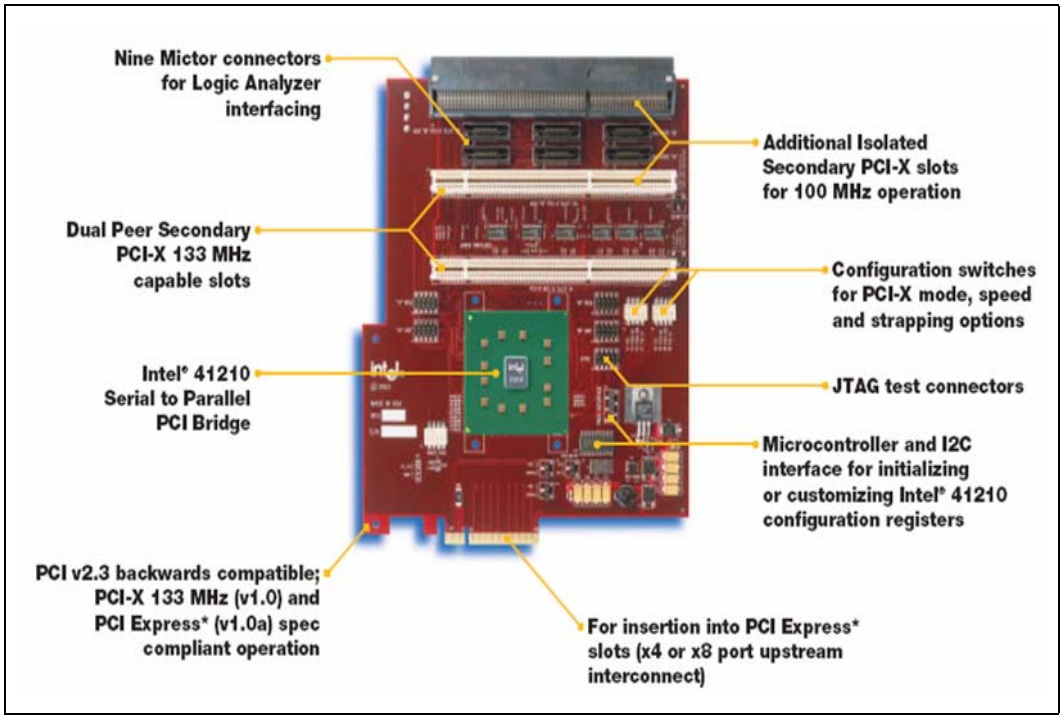
- Complies fully with:
  - Protocol and electrical standards of the *PCI Local Bus Specification*, Revision 2.3
  - *PCI-X Bridge Architecture*, Rev 1.0 B
  - *PCI-Express Base Specification*, Rev 1.0A
  - *PCI-Express Card Electrical Mechanical Specification*
  - *PCI-Express Bridge Specification.*
- Includes a 41210 "transparent" PCI-X Enhanced PCI-to-PCI Bridge that provides bridging between two processor domains.
- Includes a host PCI-Express interface that plugs into any x8 PCI-Express option card slot.
- Provides dual peer PCI-X 133 MHz slots on separate bus segments in addition to each having a segregated PCI-X100/66 MHz slot
- Three MICTOR LA connectors for logic analyzer interfacing of each bus segment
- Support, Products, and Documentation

4.0 Major Components

The major components for the 41210 Bridge include:

- For the A Secondary:
  - — J11 is the PCI-X 100/66 MHz card slot.
  - — J7 is the PCI-X 133 MHz card slot.
- For the B Secondary:
  - — J12 is the PCI-X 100/66 MHz card slot.
  - — J8 is the PCI-X 133 MHz card slot.
- MICTOR connectors U14-17 and U19-20 provide test points for the 64-bit S_AD signals.
- Header Connectors J3 and J4 provides test points for the PCI Bus A REQ/GNT signals.
- Header Connectors J5 and J6 provides test points for the PCI Bus B REQ/GNT signals.
- J1 is the JTAG connector.
- J15 provides access to the Microcontroller
- S1, S3, S4, are option switches.

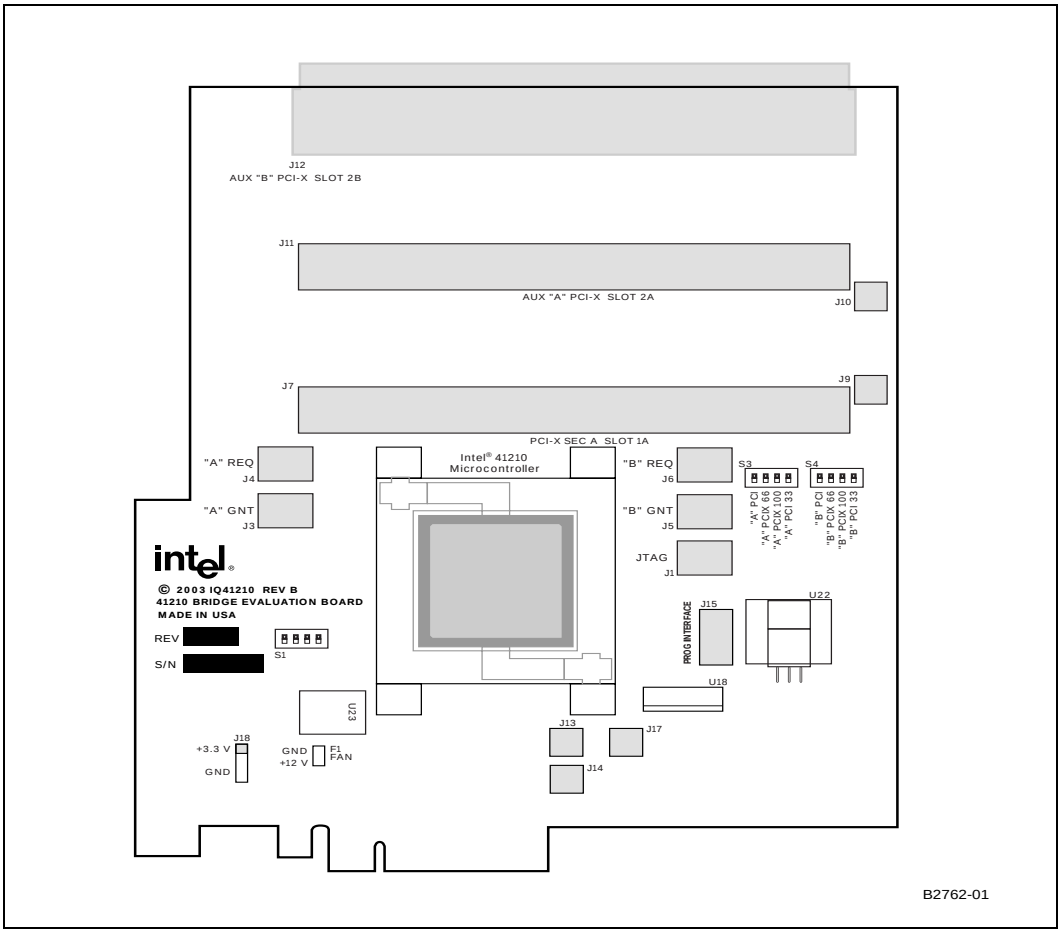
Figure 1. Major Components Overview



5.0 DIP Switches

The 41210 Bridge uses a combination of switches and jumpers to control the various configuration options. The following sections describe these controls.

Figure 2. Switches, Jumpers, and Connectors Location



5.0.1 Switch Settings

Table 1 and Table 2 describe the functions of the 41210 Bridge Evaluation Board switches. The switches should be set before powering up the system. Figure 2 shows the Evaluation board switches.

Note: When a switch is ON, it is Closed.

Table 1. DIP Switch Operation, PCI-X and PCI Clock Frequency

Switch	Function	Pos 1	Pos 2	Pos 3	Pos 4
S3	Selects Secondary A PCI-X 133 MHz	Open	Open	Open	NA
S3	Selects Secondary A PCI-X 100 MHz	Open	Open	Closed	NA
S3	Selects Secondary A PCI-X 66 MHz	Open	Open	Closed	NA
S3	Selects Secondary A PCI 66 MHz	Closed	NA	NA	Open
S3	Selects Secondary A PCI 33 MHz	Closed	NA	NA	Closed
S4	Selects Secondary B PCI-X 133 MHz	Open	Open	Open	NA
S4	Selects Secondary B PCI-X 100 MHz	Open	Open	Closed	NA
S4	Selects Secondary B PCI-X 66 MHz	Open	Open	Closed	NA
S4	Selects Secondary B PCI 66 MHz	Closed	NA	NA	Open
S4	Selects Secondary B PCI 33 MHz	Closed	NA	NA	Closed

Table 2. DIP Switch Operation, SMBUS ADRESS

Switch	Function	Pos 1-4
S1	All 1's	Open
S4	***All 0's***	***CLOSED***

Note: ***BOLD*** settings are Defaults.

5.1 Jumpers

In addition to the DIP switches, the 41210 Bridge provides stake-pin jumpers for selecting special features. The jumpers can be used for debugging and for evaluating special features. Table 3 through Table 8 show the configuration jumpers and the jumper function. Figure 2 shows the 41210 Evaluation Board jumpers.

Table 3. Jumper Connections, JTAG Port

Jumper	Function	Default
J1-2,1	TCK Test Clock	***Not Installed***
J1-4,3	TDO Test Data Out	***Not Installed***
J1-6,5	TDI Test Data In	***Not Installed***
J1-8,7	TMS Test Mode Select	***Not Installed***
J1-10,9	TRST# Test Reset	***Not Installed***
J1-1,3,5,7,9	GND	
J1-11,12	NC	

Table 4. Jumper Connections, Microcontroller I2C interface

Jumper	Function
J15-1	MPP/CLR
J15-2	VDD
J15-3	GND
J15-4	RB(7) (dat)
J15-5	RB(6)(Clk)
J15-6	nc

Table 5. Jumper Connections, GNT “A” and “B” Header

Jumper	Function	Position	Default
J3 & 5-1,2	GNT4	1	Not Installed
J3 & 5-3,4	GNT3	2	Not Installed
J3 & 5-5,6	GNT2	3	Installed
J3 & 5-7,8	GNT1	4	Installed
J3 & 5-9,10	GNT0	5	Installed
J7-2,4,6,8,10	GND		
J7-11,12	NC		

Table 6. Jumper Connections, REQ “A” and “B” Header

Jumper	Function	Position	Default
J4 & 6-1,2	REQ4	1	Not Installed
J4 & 6-3,4	REQ3	2	Not Installed
J4 & 6-5,6	REQ2	3	Installed
J4 & 6-7,8	REQ1	4	Installed
J4 & 6-9,10	REQ0	5	Installed
J7-2,4,6,8,10	GND		
J7-11,12	NC		

Table 7. Jumper Connections, J13, J14 and J17

Function	Normal Installed	Test mode
SMDAT	J13-1 to J13-2	J13-2 to J13-3
SMCLK	J14-1 to J14-2	J14-2 to J14-3
CFGRETRY	J17-1 to J17-2	J17-2 to J17-3

Note: When selecting External Oscillator Source, source can be connected to the J8 BNC.

Note: ***BOLD*** settings are Defaults.

Table 8. Jumper Connections, QSWITCH EN Header

Function	Installed	Not Installed
For 133 MHz Operation	J9 &10-1 to J9 &10-2	J9 &10-3
Enables 2nd PCI/PCI-X Connector & MICTOR LA Connectors	***J9 &10-2 to J9 &10-3***	***J9 &10-1***

Note: J9 and J10 straps the QSWITCHEN# line.

Note: ***BOLD*** settings are Defaults.